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easily **integrated** into the schedder. Section 5 compues to existing approaches and in Section 6 experimentd **....** are used M **common** exit points for all exit-statements within a loop. **...** It can be defined as a **subgraph CFG**(V, E \ Ed,,) of the CDFG. **.....** **Scheduling** Algorithm For Control-Dominated. **Circuits**," in **...**
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Figure 5 shows an example ILP vs. code size curve, which exhibits **common ....** treegion, which is a single-entry multiple-exit **sub-graph** of control flow graph (**CFG**) of a program, is **.....** Trans. on CAD of **Integrated Circuits** and Systems, 13(4), 1994. **...** **scheduling** of **subgraphs**", Proc. 32nd Ann. Int'l Symp. **...**
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into a suitable set of customized **integrated circuits**, to a full software implementation, where all the tasks are implemented **....** 4) **scheduling** of the CFSM's and generation of the RTOS; **....** the original specification (e.g., **CFG** graph). However, the **....** compact (reduced) by sharing **common** functional **subgraphs**. **...**
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that (l, u) and (r, u)∈Ed; a **CFG**-feature is a **subgraph** S = **..... Integrated Circuits** and Systems, 15(8), pages 877–888, 1996. [9] P. Bonzini and L. Pozzi. **...**
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Mar 12, 2006 **...** [7] **integrated** a fairly accurate energy estimation engine in the **... Common** examples are Altera Nios II processor [13], LEON processor [12], etc. **.... subgraph** by ISE. **CFG**/DFG w/ ISEs. **Scheduling**. Register Alloc **.....** more **circuit** activity, an initial expectation is increased power with the addition **...**
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In this paper, we present an **integrated** framework that drives a design flow from an application to a **.... CFG**/DFG and returns **subgraphs** or ISEs that would maxi- **.... scheduling**, register allocation and target code generation as a back-end pass. **.....** and AFU apparently indicates more **circuit** activity, an ini- **...**
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**common subgraph** extraction, which exploits only sim- ilarities represented by the largest **common subgraph**. .... order to enable a straightforward operation **scheduling**. .... Design of **Integrated Circuits** and Systems, vol. 24, no. 7, **...**
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Aug 14, 2003 **...** Each subroutine is mapped to a separate **subgraph**. **...** The original program **CFG** The encoded **CFG** The Eulerian **circuit** 1 2 3 **...** Another major problem results from the sharing of the WDP stack as a **common** re- source between different processes. **...** the WDP is **integrated** into this communication system, **...**
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graphs of the **CFG**. These **subgraphs** are identified according to the requirements of **...** tion can be solved by well-known methods of Eulerian **circuit** generation. **.....** off-the-shelf highly **integrated** boards; so the instruction bus of the processors is not ob- **...** guards, **scheduler** informations) and **common** signatures. **...**
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Aug 23, 2007 **...** From two or more Data Flow Graphs, a largest **common subgraph** is determined. **...** In a method of making an **integrated circuit** for use as a **...**
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